3U VPX Module Xilinx VERSAL ACAP with FMC+

Overview

PanaTeQ's **VPX3-VERSA1** is a 3U OpenVPX module based on the **VERSAL A**daptative **C**ompute **A**cceleration Platform (**ACAP**) device from Xilinx. It support both the **Prime** and **AI Core** series.

The VERSAL integrates a Dual-core ARM Cortex-A72 based Application Processing Unit (**APU**), a Dual-core ARM Cortex-R5F based Real-Time Processing Unit (**RPU**), DSP Engines, AI Engines (VC devices only) and a large Programmable Logic (**PL**) in a single device. It also includes on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces.

The board can be ordered with different versions of the VERSAL family of devices, coupled up to 8GB 64-bit DDR4-3200 Processing Memory with 8-bit ECC.

Up to 8GB 64-bit of DDR4-3200 is also available as the Programmable Logic Memory, allowing data streaming applications such as video CODEC and signal processing. 128GB of soldered eMMC managed NAND Flash is available for local data storage.

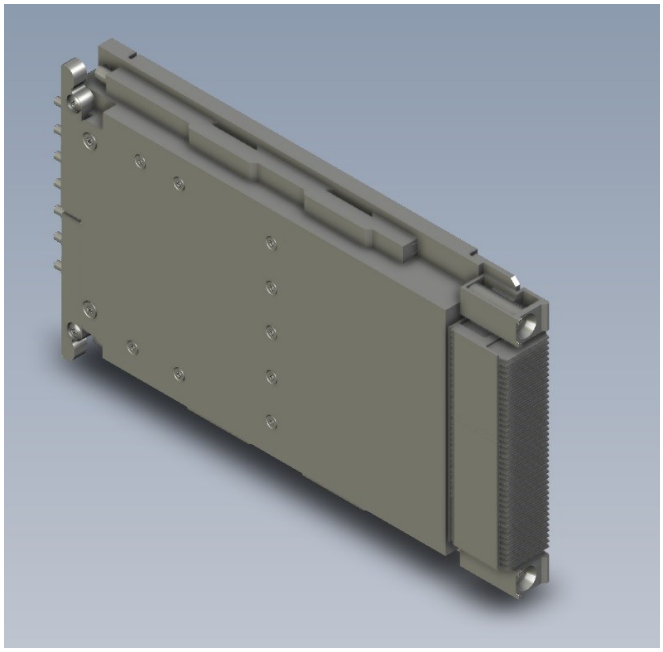
The VPX3-VERSA1 uses advanced DC/DC power modules from Linear Technology using PMBus and PanaTeQ's **Smart Power Management** technology.

For frond-end I/O interfaces, an on-board **FMC+** site compliant to the Vita 57.4 HPC standard with 180 SE IO (90 Diff Pairs) and up to 16 MGT, allowing a wide range of applications such as EW warfare systems, High-Speed Communication, LIDAR/RADAR/SONAR.

The board can act as a **Single Board Computer** in the VPX system. When the VPX3-VERSA1 is System Controller, there is no need to add any SBC in the VPX System, improving **S**ize, **W**eight, **P**ower and **C**ost (SWaP-C).

A large number of the peripherals are available on the VPX backplane: 2x ETH 1000Base-T, 2x USB 2.0, 4x RS-232/422/485, 20x GPIOs.

The air cooled PanaTeQ System Development Kit **VPX3-VERSA1-PSDK** is available for the developers and includes a lab chassis with 5-slots Full-Mesh backplane, the VPX3-VERSA1-C1N-AS and RTM-VERSA1 boards, a PentaLinux BSP, PanaTeQ FPGA Design Kit (**PAN-FDK**) and cables.



Key Features

- 3U VITA 46.0, 46.4, 46.6, 65.0 Compliant
- Optional **SOSA** version **VPX3-VERSA1S** (Contact Us)
- Xilinx VERSAL AI Core and Prime Series based
- VC1802/1902 and VM1302/1402/1802 VSVD1760 Package
- Dual Core Arm A72 up to 1.7 GHz
- Dual Core Arm R5F up to 750 MHz
- DSP Engines up to 1968
- AI Core Enines up to 400
- Up to 8GB DDR4-3200 64-bit PS memory with 8-bit ECC
- Up to 8GB DDR4-3200 64-bit PL memory
- eMMC 128GB, MRAM 512KB
- 8x MGTs on VPX-P1, PCIe Gen3 support
- 2x ETH 1000Base-X/SGMII on VPX-P1 Control Plane
- 20x GPIOs on VPX-P1
- 2x ETH 1000Base-T on VPX-P2
- 4x RS.232 or 2x 422/485 on VPX-P2
- 2x USB 2.0 on VPX-P2
- FMC+ VITA 57.4 site with 180x IOs, up to 16x MGT
- Optional 4x Full-Duplex Optical Links VITA 66.4 or 66.5
- Smart Power Management using DC/DC with PMBus
- Board Management Controller ARM Cortex-M3 based
- VPX System Controller
- Air Cooled and Conduction Cooled
- KVPX Connectors in option

Typical Applications

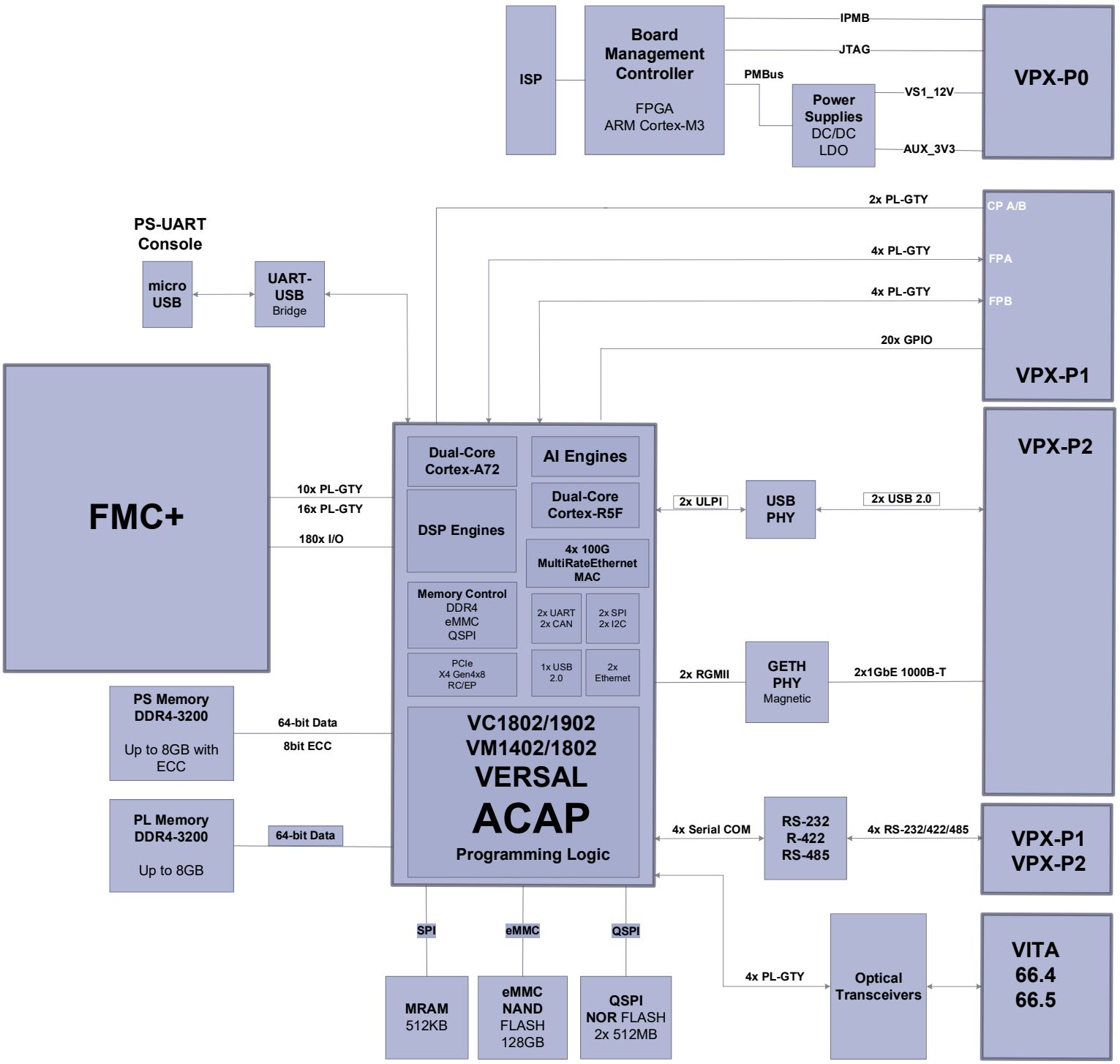
- MILCOM, Software Defined Radio, MIMO
- Situational Awareness Systems
- Electronic Warfare, Signal Intelligence
- LIDAR/RADAR/SONAR Systems
- Advanced Multi-Axes Motors Control

VITA Open Standards, Open Markets

OpenVPX™

FMC+™

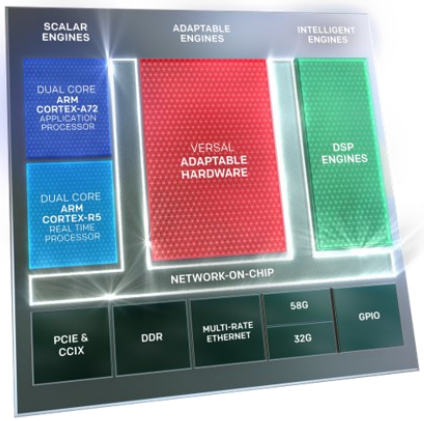
Block Diagram



Xilinx VERSAL Adaptative Compute Acceleration Platform (ACAP) Overview

VERSAL AI Core Series

VERSAL Prime Series



Architecture

Versal ACAPs are built around an integrated shell composed of a programmable network on chip (NoC), which enables seamless memory-mapped access to the full height and width of the device. ACAPs comprise: a multicore scalar processing system (PS); an integrated block for PCIe® with DMA and Cache Coherent Interconnect Designs (CPM); SIMD VLIW AI Engine accelerators for artificial intelligence and complex signal processing; and Adaptable Engines in the programmable logic (PL). Together, these form a platform for fast time-to-market (TTM) compute acceleration for cloud, edge, and networking applications. The platform management controller (PMC), adjacent to the PS, is responsible for booting and configuring the device. Versal devices typically have I/O and memory controllers on the north and south edges of the device and serial transceivers on the east and west edges. The NoC spans full height and width of the device.

Compute and Acceleration

The Versal AI Core series has an array of signal processing cores that are highly optimized for functions in machine learning, convolutional neural networks, wireless radio, backhaul, cable, and radar applications. The array consists of a number of AI Engines, each comprising a 32-bit scalar RISC processor, fixed and floating point vector units, data memory, and interconnect. AI Engines can be used as a single tile, as the complete array, or at any granularity in between. The creation of custom acceleration and compute engines in the AI Engine array is done at a high-level through C and C++.
Every Versal ACAP has Scalar Engines that comprise a dual-core Arm® Cortex®-A72 (APU) and a dual-core Arm Cortex-R5F (RPU) in the PS. The PS includes a number of peripherals for communication standards, including gigabit Ethernet and USB 2.0, and controllers for SPI, I2C, UART, and CAN-FD. The PS accesses the DDR memory controllers on the top and bottom of the device through the NoC. In addition to interfacing to external memory, the APU includes: Level 2 (L2) cache; the RPU includes tightly coupled memory (TCM); and both APU and RPU have access to the on-chip memory (OCM). The PL is made up of configurable logic blocks, containing 6-input look-up tables (LUTs) and flip-flops; different-sized memory blocks; 36Kb block RAM and 288Kb UltraRAM; digital signal processing (DSP) blocks; and a wealth of interconnect, switches, and muxes to connect blocks together. All resources are arranged in columns. The PL is divided into regions that are a fixed height. Each region has its own clocking capabilities and NoC access points.

Platform Management

The PMC resides adjacent to, but is independent from, the PS. It is responsible for the boot and configuration of the device from the primary boot source. The PMC is also responsible for configuring the PL, which can be configured before or after the PS. It also controls encryption, authentication, system monitoring, and device debug capabilities of the platform.

Connectivity

The south edge of the Versal ACAPs typically contains a number of XPIO banks and associated memory controllers to read from and write to DDR4 and LPDDR4 memory. XPIO can be used independently from the dedicated memory controllers for many functions, including any with soft memory controllers created in the PL. The east and west edges of the device typically contain serial transceivers capable of communicating up to 112Gb/s. The PL can also contain integrated blocks for high-value functions, such as the integrated block for PCIe (PL PCIE) with support for Compute Express Link (CXL), multirate Ethernet MAC, 600G Ethernet MAC, 600G Interlaken, and 400G High-Speed Crypto (HSC) Engine.

Board Specifications

3U VPX Interfaces

- VITA 46.0/46.4/46.6/65.0 VPX/OpenVPX Specifications compliant
- 8x MGT connected to/from VERSAL device. PCIe 8x Gen4 support
- 2x1000BASE-X/SGMII links on VPX Control Plane
- 2x1000BASE-T, 4x RS-232/422/485, 2x USB 2.0, 20x GPIOs
- Optional 4x Full-Duplex Optical Links VITA 66.4 or 66.5. Please contact us for more details
- Board Management Controller (BMC) Interface. VITA 46.11 Ready
- System Controller capability
- JTAG

OpenVPX VITA 65.0 Profiles

- MOD3-PAY-8U-16.2.9-1, MOD3-PAY-8U-16.2.9-2
- MOD3-PAY-2F4F2U-16.2.10-3, MOD3-PAY-2F4F2U-16.2.10-4
- Optional 4x Full-Duplex Optical Links VITA 66.4 or 66.5. Please contact us for more details

Xilinx VERSAL ACAP

- Supported Devices:**VM1402** / **VM1802** / **VC1802** / **VC1902** VSVD1760 Package (Speed Grade –1/2)
- Processing System : Dual-Core ARM A72, Dual-Core ARM R5F, 2x USB, 2x GETH MACs
- Programmable Logic: 1238K Logic Cells (VM1402) / 1586K Logic Cells (VM1802)
  1968K Logic Cells (VC1802) / 1968K Logic Cells (VC1902)
- On-Chip Memories: 137Mb (VM1802) / 141Mb (VM1802) / 191Mb (VC1802) / 191Mb (VC1902)
- DSP Engines: 1698 (VM1402) / 1600 (VM1802) / 1968(VC1802) / 1968 (VC1902)
- AI Engines: N/A (VM1402) / N/A (VM1802) / 300 (VC1802) / 400 (VC1902)
- High Speed Serial Links: up to 24 full duplex, high performance, GTY Multi-Gigabit Tranceivers (MGT) @ up to 32.75 Gb/s
- Supported by PanaTeQ's FPGA Development Kit (**PAN-FDK**)

External Memories

- Up to 8GB of DDR4-3200 Processor System (PS) memory, 64-bit data, 8-bit ECC
- Up to 8GB of DDR4-3200 Programmable Logic (PL) memory, 64-bit data, no ECC
- 128GB eMMC of managed NAND Flash memory. HS200 support @ up to 100MB/s
- 512KB of SPI MRAM (NVRAM)
- 2x 2Gb of QSPI NOR Flash memory for booting VERSAL Programmable Logic and Firmware Processing System

VITA 57.4 FMC+ Slot

- Compliant to the VITA 57.4 specification
- Up to 16x high-performance MGT to/from VERSAL Programmable Logic
- 180x LVCMOS or 90x LVDS to/from VERSAL Programmable Logic
- 2x clocks FMC to VERSAL Programmable Logic
- 2x clocks FMC to VERSAL MGT
- 2x bidirectional clocks

Board Management Controller (BMC)

- .Based on Microsemi SmartFusion Customizable System-on-Chip (**cSoC**) with on-chip ARM Cortex-M3 at up to 100MHz
- Real-Time Monitoring+Alarms: Voltages, Currents, Temperatures, 6-Axis Accelerometer, Magnetometer and Humidity
- Reset Management, Power-Up and Power-Down Sequencing. Buit-In Test (**BIT**)
- Watchdogs (Avionics type)
- Large private 32MB Event Log Flash Memory.
- UART communication with host using RTM-VERSA1 Rear-Transition Module
- Smart Power Management using Linear Technology DC/DC modules with Digital Power System Management
- Hardware Ready for full Vita 46.11 compliance

Environnemental Specifications

- Compliant with VITA 47 specification. Please contact PanaTeQ for more information

Product Codification

The VPX3-VERSA1 can be assembled with different versions of the VERSAL devices and various amounts of memory storage. The cooling technique et ruggedization level are also available options. The following table shows the product coding for all these options.

VPX3-VERSA1–C 1 N – AS

	Device	AI Engines	DSP Engines	System Logic Cells	Memory
A	VC1802	300	1600	1586K	141 Mb
B	VC1902	400	1968	1968K	191 Mb
C	VM1802	N/A	1968	1968K	191 Mb
D	VM1402	N/A	1696	1238K	137 Mb

	Device Speed Grade
1	Slowest
2	Fastest

	PS / PL Memory Size
N	4GB/4GB
M	8GB/8GB

	Ruggedization Level	VITA 47
AS	Air Standard	EAC4
AR	Air Rugged	EAC6
CC	Conduction Cooled	ECC3
CR	Conduction Rugged	ECC4

Ordering Information

The following product references are offered by Panateq as standard products. Other combinations of devices, speed grade, memory and cooling can be specially ordered. Please contact us for details

Reference	Device	Speed Grade	Memory PS/PL	Ruggedization Level
VPX3-VERSA1-C1N-AS	VM1802	-1	4GB/4GB	Standard Air Cooled

Reference	Description
RTM-VERSA1	Rear Transition Module for VPX3-VERSA1
VPX3-VERSA1-C1N-PSDK	VPX3-VERSA1-C1N-AS System Development Kit

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