XMC Module Xilinx Zynq UltraScale+ MPSoC

Overview

PanaTeQ's XMC-ZU1 is a XMC module based on the Zynq UltraScale+ MultiProcessor SoC device from Xilinx.

The Zynq UltraScale+ integrates a Quad-core ARM Cortex-A53 based Application Processing Unit (**APU**), a Dual-core ARM Cortex-R5 based Real-Time Processing Unit (**RPU**), a ARM MALI-400 based Graphic Processing Unit (**GPU**), a Video CODEC H.264/H.265 (**VCU**) and an UltraScale+ Programmable Logic (**PL**) in a single device. It also includes on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces.

The board can be ordered with different versions of the Zynq UltraScale+ family of devices, coupled up to 8GB 64-bit DDR4-2400 Processing Memory with 8-bit ECC.

Up to 2GB 16-bit of DDR4-2400 is also available as the Programmable Logic Memory, allowing data streaming applications such as video CODEC and signal processing. 64GB of soldered eMMC managed NAND Flash is available for local data storage.

The XMC-ZU1 uses four advanced DC/DC power modules from Linear Technology with PMBus and PanaTeQ's **Smart Power Management** technology.

For frond-end I/O interfaces, an on-board **PAN-IO** site with 60 SE IO (30 Diff Pairs) and 4 MGT, allowing a wide range of applications such as Software Defined Radio, Video Camera Processing, advanced Multi-Axes Motors controller, Multi-Gig Ethernet Communications, LIDAR/RADAR/SONAR.

The board can act as a **PrPMC** in the system. When the XMC-ZU1 is System Controller.There is no need to add any SBC in the System, improving **S**ize, **W**eight, **P**ower and **C**ost (SWaP-C).

A large number of the Zynq Ultrascale+ PS peripherals are available on the XMC connectors: 2x ETH 1000Base-T, 2x USB 3.0/2.0, 2x USB 2.0, 1x SATA 3.1, 2x CAN-2.0B, 2x RS-232/422/485, 4x MGT, 24x GPIO, Video Out Display Port 1.2.

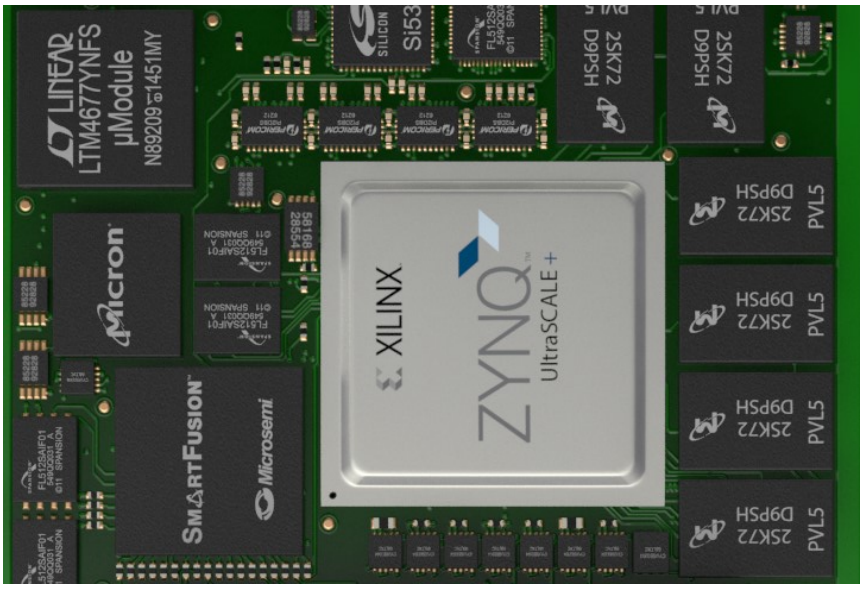
Linux and VxWorks 7 Plus BSP are supported.

Key Features

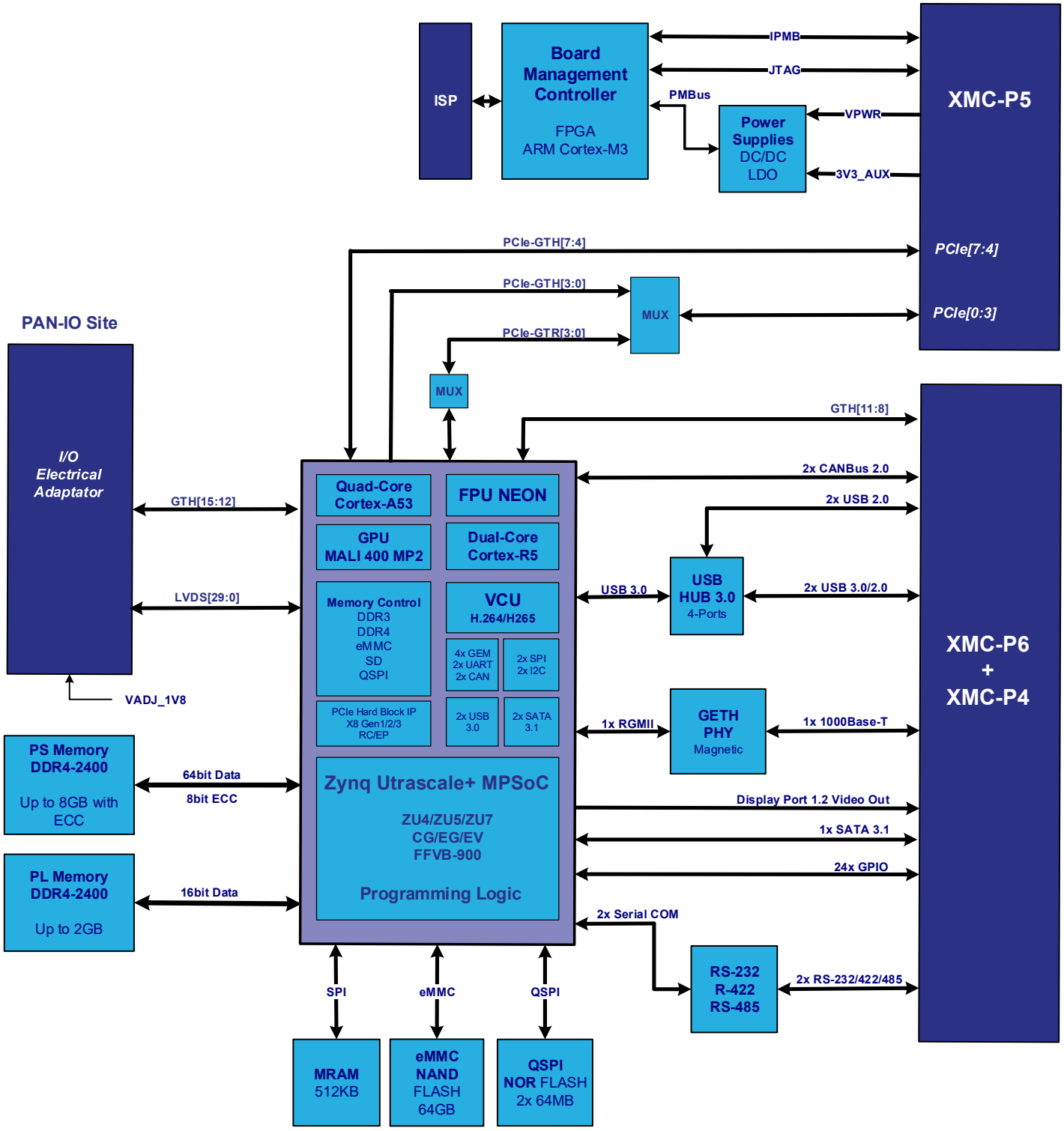
- Vita 42.3 XMC Compliant
- Xilinx Zynq UltraScale+ MPSoC
- ZU4/ZU5/ZU7 CG/EG/EV FBVB-900 Package
- Up to 8GB DDR4-2400 64-bit PS memory with 8-bit ECC
- Up to 2GB DDR4-2400 16-bit PL memory
- eMMC 64GB (V4.51), MRAM 512KB
- PCIe x8 Gen1/2/3 on XMC-P5
- 4x MGT on XMC-P6
- 1x Display Port 1.2 Video Out on XMC-P6
- 1x ETH 1000Base-T on XMC-P4
- 2x USB 3.0/2.0, 2x USB 2.0, 1x SATA 3.1 on XMC-P6
- 24x LVCMOS or 12x LVDS GPIO on XMC-P6
- 2x RS.232/422/485, 2x CAN 2.0B on XMC-P4
- PAN-IO site with 60x IO / 30x LVDS, 4x MGT
- Smart Power Management using 4x LTM467x with PMBus
- Board Management Controller ARM Cortex-M3 based
- Air Cooled and Conduction Cooled

Typical Applications

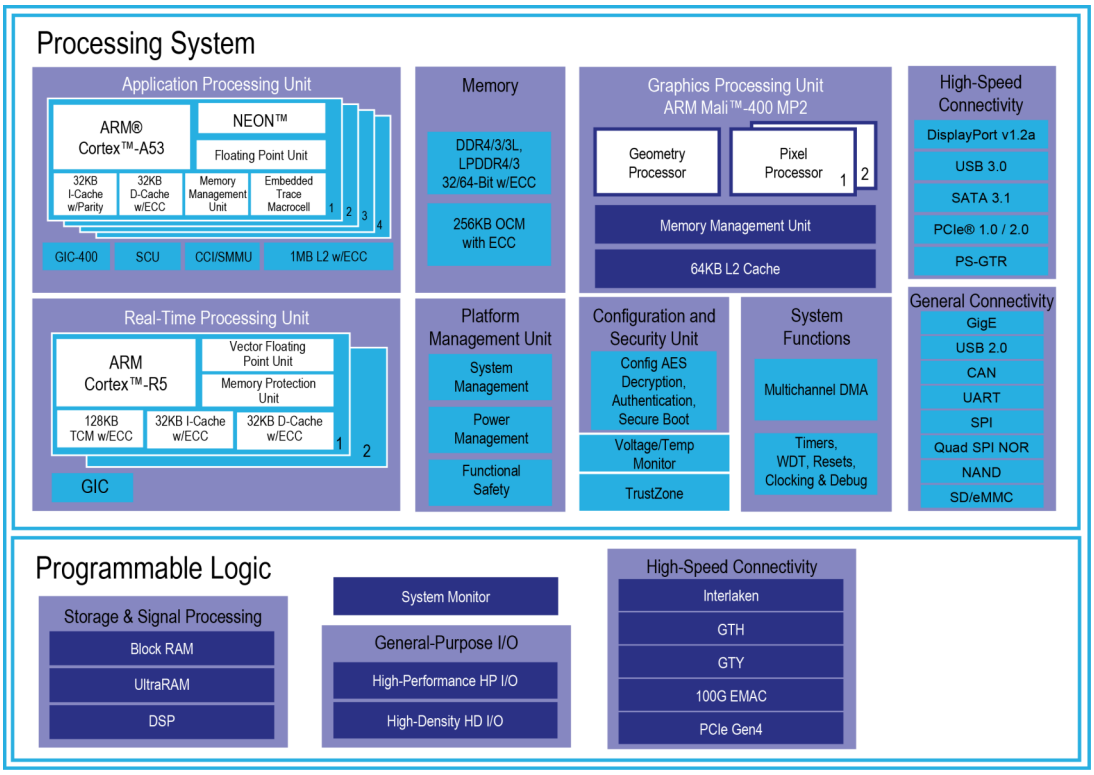
- MILCOM, Software Defined Radio, MIMO
- Situational Awareness Systems
- Electronic Warfare, Signal Intelligence
- LIDAR/RADAR/SONAR Systems
- Advanced Multi-Axes Motors Control
- Video CODEC and Signal Processing



Block Diagram



Xilinx Zynq Ultrascale+ MPSoC Processing System Highlights



Applications processing unit (APU) with quad-core ARM® Cortex™-A53 processors up to 1.5GHz:

- Next-generation ARMv8 architecture supporting 32- or 64-bit data widths
- Ideal for Linux and bare-metal SMP/AMP application systems

Real-time processing unit (RPU) with dual-core ARM Cortex-R5 processors up to 600MHz:

- Low-latency, highly deterministic performance APU offloading

New integrated hardened multimedia blocks up to 667MHz:

- Graphics processing unit (GPU) [ARM Mali™-400MP2]
- 4Kx2K 60fps video encoder/decoder (VCU)
- 4Kx2K 30fps DisplayPort interface

New integrated high-speed peripherals:

- PCIe® Gen1 or Gen2 root complex and integrated Endpoint block in x1, x2, and x4 lanes
- USB 3.0/2.0 with host, device, and OTG modes
- Gigabit Ethernet with jumbo frames and precision time protocol
- SATA 3.1 host
- Dedicated quad transceivers up to 6Gb/s

General and boot peripherals:

- CAN, I2C, QSPI, SD, eMMC, and NAND flash interfaces
- GPIO, UART, and trace ports
- 6-port DDR controller with ECC, supporting x32 and x64 DDR3, DDR3L, LPDDR3, LPDDR4, DDR4
- Integrated platform management unit (PMU) supporting multiple power domains
- Integrated configuration security unit (CSU)
- TrustZone support
- Peripheral and memory protection

Board Specifications

XMC Interfaces

- VITA 42.3 Specifications compliant
- XMC P5: 8 lanes PCIe Gen1/2/3
- XMC P6: 4x MGT GTH @ up to 16.3 Gb/s connected to/from Zynq Ultrascale+ Programming Logic
- XMC P4; 1x ETH 1000BASE-T, 2x RS-232/422/485
- XMC P6: 1x SATA 3.1, 1x Display Port 1.2 VIDEO OUT, 2x USB 3.0/2.0, 2x USB 2.0, 12x LVDS
- XMC P5: IPMI EEPROM, Temperatures, Voltages, Currents, Board Management Controller (BMC), JTAG

Xilinx Zynq Ultrascale+ MPSoC

- Supported Devices:**XCZU4 CG/EG/EV XCZU5 CG/EG/EV XCZU7 CG/EG/EV** Speed Grade –1/2/3 FBVB900 Package
- Processing System : Quad-Core ARM A53, Dual-Core ARM R5, GPU Mali-400, 2x SATA, 2x USB, 4x GETH MACs
- Programmable Logic: 192K Logic Cells (ZU4) / 256K Logic Cells (ZU5) / 504K Logic Cells (ZU7)
- On-Chip Memories: 18.5Mb (ZU4) / 23.1Mb (ZU5) / 38.0Mb (ZU7)
- DSP Slices: 728 (ZU4) / 1248 (ZU5) / 1728 (ZU7)
- High Speed Serial Links: 16 full duplex, high performance, GTH Multi-Gigabit Tranceivers (MGT) @ up to 16.3 Gb/s
- 2x 10-bit, 1MSPS ADCs for System Monitoring
- Supported by PanaTeQ's FPGA Development Kit (**PAN-FDK**)

External Memories

- Up to 8GB of DDR4-2400 Processor System (PS) memory, 64-bit data, 8-bit ECC
- Up to 2GB of DDR4-2400 Programmable Logic (PL) memory, 16-bit data, no ECC
- 64GB eMMC v4.51 of managed NAND Flash memory. HS200 support @ up to 100MB/s
- 512KB of SPI MRAM (NVRAM)
- 2x 512Mb of QSPI NOR Flash memory for booting Zynq Utrascale+ Programmable Logic and Firmware Processing System

Front I/O PAN-IO

- 4x high-performance MGT @ up to 16.3 Gb/s to/from Zynq Programmable Logic
- 60 LVCMOS_18 or 30 LVDS_18 to/from FPGA Zynq Ultrascale+ Programmable Logic
- 2x clocks FMC to Zynq Ultrascale+ Programmable Logic
- 2x clocks FMC to Zynq Ultrascale+ GTH Transceivers
- VADJ = 1V8 (default). 2V5 not supported by Zynq Ultrascale+ HP Banks

Environnemental Specifications

- Commercial Ruggudized 0-50C
- Conduction Cooled –40C to 70C at Thermal Interface

Product Codification

The XMC-ZU1 can be assembled with different versions of the Zynq Ultrascale+ devices and various amounts of memory storage. The cooling technique et ruggedization level are also available options. The following table shows the product coding for all these options.

XMC-ZU1–B 1 N –AS

	Device	ARM A53 Cores	GPU	Video CODEC	System Logic Cells	DSP Slices	Memory
A	XCZU4CG	2	No	No	192K	728	18.5 Mb
B	XCZU5CG	2	No	No	256K	1248	23.1 Mb
C	XCZU7CG	2	No	No	504K	1728	38.0 Mb
D	XCZU4EG	4	Yes	No	192K	728	18.5 Mb
E	XCZU5EG	4	Yes	No	256K	1248	23.1 Mb
F	XCZU7EG	4	Yes	No	504K	1728	38.0 Mb
G	XCZU4EV	4	Yes	Yes	192K	728	18.5 Mb
H	XCZU5EV	4	Yes	Yes	256K	1248	23.1 Mb
I	XCZU7EV	4	Yes	Yes	504K	1728	38.0 Mb

	PS / PL Memory Size
N	2GB/512MB
M	4GB/1GB
P	8GB/2GB

	Device Speed Grade
1	Slowest
2	Mid
3	Fastest

	Ruggedization Level	VITA 47
AS	Air Standard	EAC4
AR	Air Rugged	EAC6
CC	Conduction Cooled	ECC3
CR	Conduction Rugged	ECC4

Ordering Information

The following product references are offered by PanaTeQ as standard products. Other combinations of devices, speed grade, memory and cooling can be specially ordered. Please contact us for details

Reference	Device	Speed	Memory	Ruggedization Level
XMC-ZU1-G1M-AS	ZU4EV	-1	4GB/1GB	Standard Air Cooled
XMC-ZU1-G1M-CC	ZU4EV	-1	4GB/1GB	Conduction Cooled
XMC-ZU1-H1M-AS	ZU5EV	-1	4GB/1GB	Standard, Air Cooled
XMC-ZU1-H1M-CC	ZU5EV	-1	4GB/1GB	Conduction Cooled
XMC-ZU1-I1M-AS	ZU7EV	-1	4GB/1GB	Standard, Air Cooled
XMC-ZU1-I1M-CC	ZU7EV	-1	4GB/1GB	Conduction Cooled

Reference	Description
PAN-IO-A1	Front I/O Module for XMC-ZU1 (Please contact us)
XMC-ZU1-PDSK	XMC-ZU1 Development System Kit (Please contact us)

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