

# VPX3-ZU1-SDR-B 3U VPX Zynq Ultrascale+ AD9375 SDR System Development

## Overview

The VPX3-ZU1-SDR-B is a 3U OpenVPX System Development based on PanaTeQ's VPX3-ZU1 Zynq Ultrascale+ and FMC-ZU1RF-B module for Software Defined Radio applications.

The kit includes the following items:

- An air-cooled 4U desktop chassis with 5-slots VPX Full-Mesh backplane with 250W PSU.
- VPX3-ZU1-B1N-AS: 3U OpenVPX Zynq Ultrascale+ with FMC Site module.
- RTM-ZU1-A1: Rear Transition Module for the VPX3-ZU1.
- FMC-ZU1RF-B-W1A-AS: FMC Wideband RF Transceiver AD9375 based.
- A Petalinux/Yocto Linux BSP

## Key Features

### VPX3-ZU1-B1N-AS module

- 3U OpenVPX module, Air-Cooled
- Xilinx Zynq Ultrascale+ ZU9G-1FFVC900E
- 2GB PS DDR4-2400 memory 64-bit, 8-bit ECC
- 512MB PL DDR4-2400 memory 16-bit, no ECC
- 64 GB eMMC managed NAND Flash
- FMC HPC site with 10x MGTs @ up to 16.3Gb/s

### FMC-ZU1RF-B-W1A-AS module

- Fully ADRV9375 evaluation board compatible
- Dual Transmitter (Tx), Dual Receiver (Rx)
- Observation Receiver (ORx) with 2 inputs
- Fully integrated, ultralow power DPD actuator and adaptation engine for PA linearization
- Sniffer Receiver (SnRx) with 1 input
- TX Ext LO Input/Output, RX Ext LO Input/Output
- Reference Clock Input
- RF Coverage 300MHz to 6.0 GHz
- Linearization signal BW to 40 MHz
- Tx Synthesis Bandwidth (BW) to 250 MHz
- Rx Bandwidth: 7MHz to 100 MHz
- On-Board VCXO @ 122.88 MHz.
- For other options, please contact us

### RTM-ZU1-A

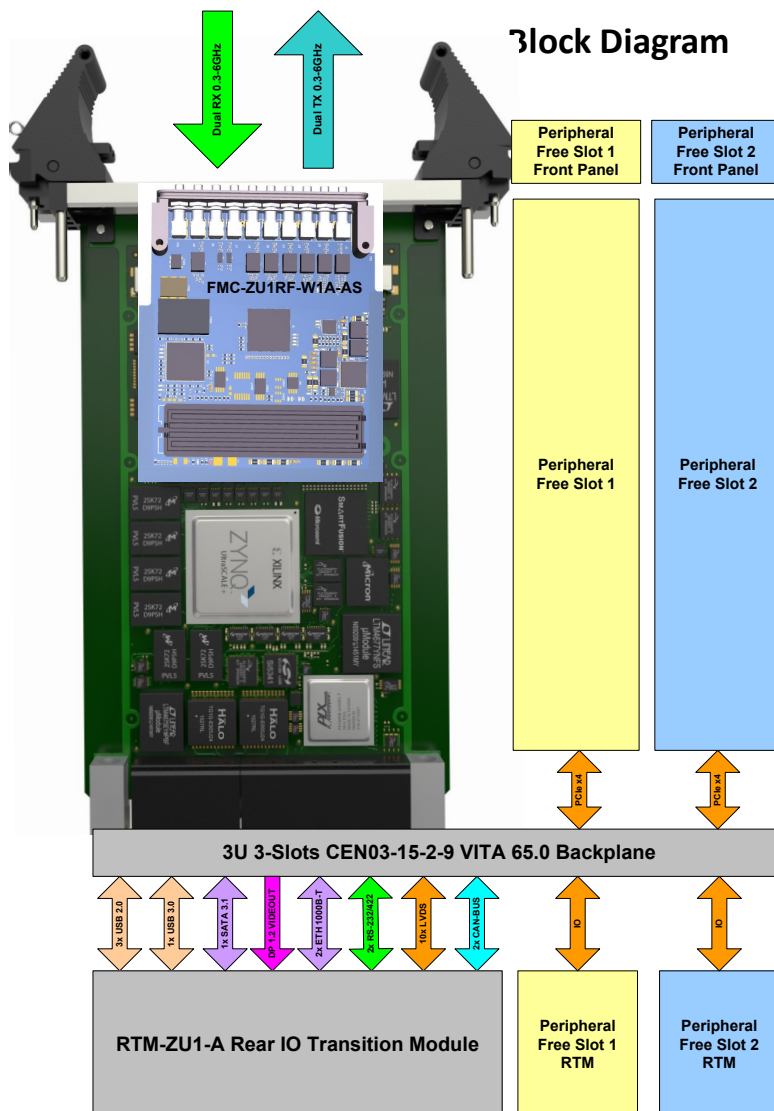
- Rear Transition Module for VPX3-ZU1 module
- 2x 100/1000Base-T RJ-45
- 2x USB 2.0 Type-A, 2x USB 3.0 Type-A
- 1x SATA 3.1, 1x mini DisplayPort

### Desktop Chassis

- 4U Compact Desktop Chassis
- AC/DC Input PSU 250W, Air Cooled
- 5-Slots Vita 46.0 VPX Full-Mesh backplane.
- 0.8 Inch Slot Pitch
- Support Rear I/O Through RTMs on each Slots
- For other options, please contact us

### Software & VHDL Support

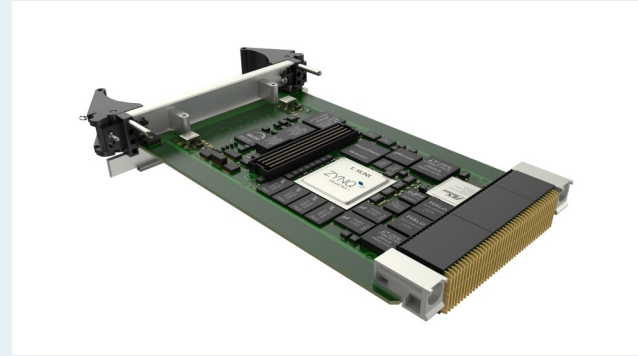
- Petalinux/Yocto BSP
- PanaTeQ FPGA Design Kit (PAN-FDK)



# VPX3-ZU1-SDR-B SDR System Development Kit Specifications

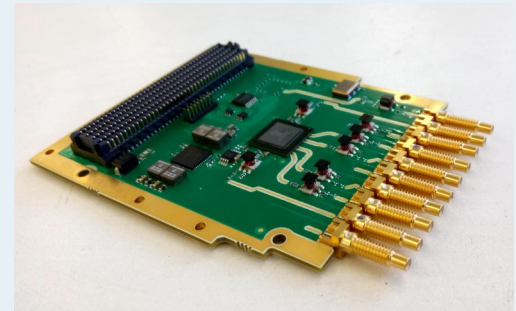
## VPX3-ZU1-B1N-AS

- VITA 46.0 65.0 VPX/OpenVPX specifications compliant
- Xilinx Zynq Ultrascale+ ZU9G, FFVC900, Speed Grade -1
- 2GB PS DDR4-2400 memory 64-bit, 8-bit ECC
- 512MB PL DDR4-2400 memory 16-bit, no ECC
- 64GB eMMC managed NAND Flash
- 2x1000BASE-T, 2x RS-232/422/485, 2x USB 2.0, 2x USB 3.0 on VPX
- 1x SATA 3.1, 2x CAN 2.0B, 2x RS-232/422/485 on VPX
- 1x Display Port 1.2 Video Out on VPX
- VITA 57.1 FMC HPC site, 10x MGT, 45 Diff Pairs (LA[33:0] + HA[10:0])
- Board Management Controller (BMC) Interface VITA 46.11 Ready



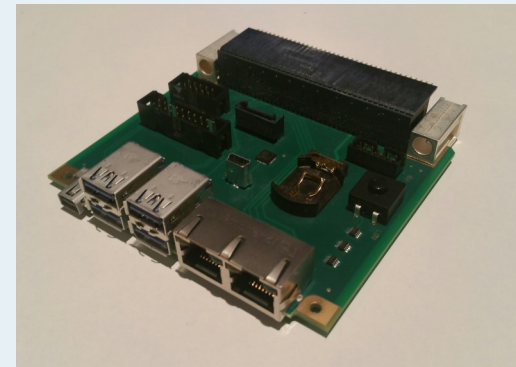
## FMC-ZU1RF-B-W1A-AS

- FMC HPC based on AD9375 Wideband RF Transceiver from Analog Device Inc.
- Fully ADRV9375 evaluation board HW/SW compatible
- Dual Transmitters (Tx), Dual Receivers (Rx)
- Observation Receiver (ORx) with 2 inputs
- Sniffer Receiver (SnRx) with 1 input
- TX Ext LO Input/Output, RX Ext LO Input/Output
- Reference Clock Input
- RF Coverage 300MHz to 6.0 GHz
- Tx Synthesis Bandwidth (BW) to 250MHz
- Rx Bandwidth: 7MHz to 100MHz
- On-board VCXO : 122.88 MHz (For other values, please contact us)



## RTM-ZU1-A1

- 2x 100/1000BaseT RJ-45 with Link Activity Leds Rear Panel connectors
- 1x mini Display Rear-Panel connector
- 4x USB 3.0/ 2.0 Type-A dual-stacked Rear-Panel connectors
- 1x SATA 3.1 vertical on-board connector
- 2x CANBus 2.0B pin-header on-board connector
- 20x GPIO 3M flat-cable on-board connector
- 2x RS-232/422/485 pin-header on-board connector



## Desktop Chassis

- Mechanical: W=180mm, H= 4U, D= 275mm
- Cooling: Air Cooled
- 5-Slots 0.8 inch Full-Mesh 3U VPX Vita 46.0 backplane
- RTM support, 250W PSU, Air Cooled
- For other VITA 65.0 Backplane profile and PSU, please contact us



## Software & VHDL

- PetaLinux/Yocto BSP
- PanaTeQ FPGA Design Kit (PAN-FDK)

## Cables

- Video mini DisplayPort to standard HDMI adaptor, SATA, USB

## Ordering Information

- VPX3-ZU1-SDR-B : VPX3-ZU1 AD9375 SDR System Development Kit  
For other configuration requests, please contact us.

## Contact Information

info@panateq.com