3U VPX AMD VERSAL RF Module

Overview

PanaTeQ's **VPX3-VERSA-RF-A** is a 3U VPX module based on the **VERSAL RF A**daptative **C**ompute **A**cceleration Platform (**ACAP**) device from AMD. It support the **RF** series **VR1602** or **VR1652** devices.

The VERSAL RF integrate a Dual-core ARM Cortex-A72 based Application Processing Unit (**APU**), a Dual-core ARM Cortex-R5F based Real-Time Processing Unit (**RPU**), **AI** Engines, **DSP** Engines and a large Programmable Logic (**PL**) in a single device. It also includes on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces.

The VERSAL RF integrate up to eight 14-bit (with calibration), 32 GSPS RF-ADCs with hard DUC and DDC IP enable fast, high resolution, flexible wide-spectrum characterization.
Eight 14-bit (with calibration), 16 GSPS RF-DACs provide RF transmit functions.
18 GHz I/O instantaneous bandwidth enables a wider input frequency pipe.

The board can be ordered with different versions of the VERSAL RF family of devices, coupled up to 4 or 8GB 64-bit DDR4-3200 Processing Memory with 8-bit ECC.

2GB 32-bit of LPDDR4-2133 is also available as the Programmable Logic Memory, allowing data signal processing.

256GB of soldered eMMC managed NAND Flash is available for local data storage.

The VPX3-VERSA-RF-A uses advanced DC/DC power modules from Linear Technology using PMBus and PanaTeQ's **Smart Power Management** technology.

The board can act as a **Single Board Computer** in the VPX system. When the VPX3-VERSA-RF-A is System Controller, there is no need to add any SBC in the VPX System, improving **S**ize, **W**eight, **P**ower and **C**ost (SWaP-C).

A large number of the peripherals are available on the VPX backplane: 1x ETH 1000Base-T, 1x USB 2.0, 4x RS-232 or 2x Full-Duplex RS-422, 16x GPIOs, 2x CAN-FD.

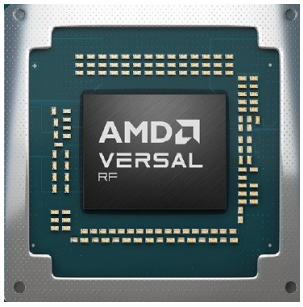
The air cooled PanaTeQ System Development Kit **VPX3-VERSA-RF-A-PSDK** is offered for the developers.

Key Features

- 3U VITA 46.0, 46.4, 46.6, 65.0 Compliant
- **SOSA Aligned** version **VPX3-VERSA-RF-AS**
- AMD VERSAL RF Series based
- VR1602/VR1652 VSVG1596 Package
- Dual Core Arm A72 up to 1.7 GHz
- Dual Core Arm R5F up to 750 MHz
- AI Engine Tiles 126
- DSP Engines 2256
- 4 or 8GB DDR4-3200 64-bit PS memory with 8-bit ECC
- 2GB LPDDR4-2133 32-bit PL memory
- 512MB (2x 2Gb) QSPI NOR, eMMC 256GB, MRAM 512KB
- 8x MGTY on VPX-P1, PCIe x4 Up to Gen5 support
- 2x ETH 1000Base-X/SGMII on VPX-P1 Control Plane
- 16x GPIOs on VPX-P2
- 1x ETH 1000Base-T on VPX-P2
- 4x RS232 or 2x Full-Duplex RS422 on VPX-P2
- 1x USB 2.0 on VPX-P1
- Optional 4x Full-Duplex Optical Links VITA 66.4 or 66.5
- Optional Front-End connector or Backplane VITA 67.3 nanoRF
- Smart Power Management using DC/DC with PMBus
- Board Management Controller ARM Cortex-M3 based
- VPX System and IPMI controllers
- Air Cooled and Conduction Cooled
- KVPX Connectors in option

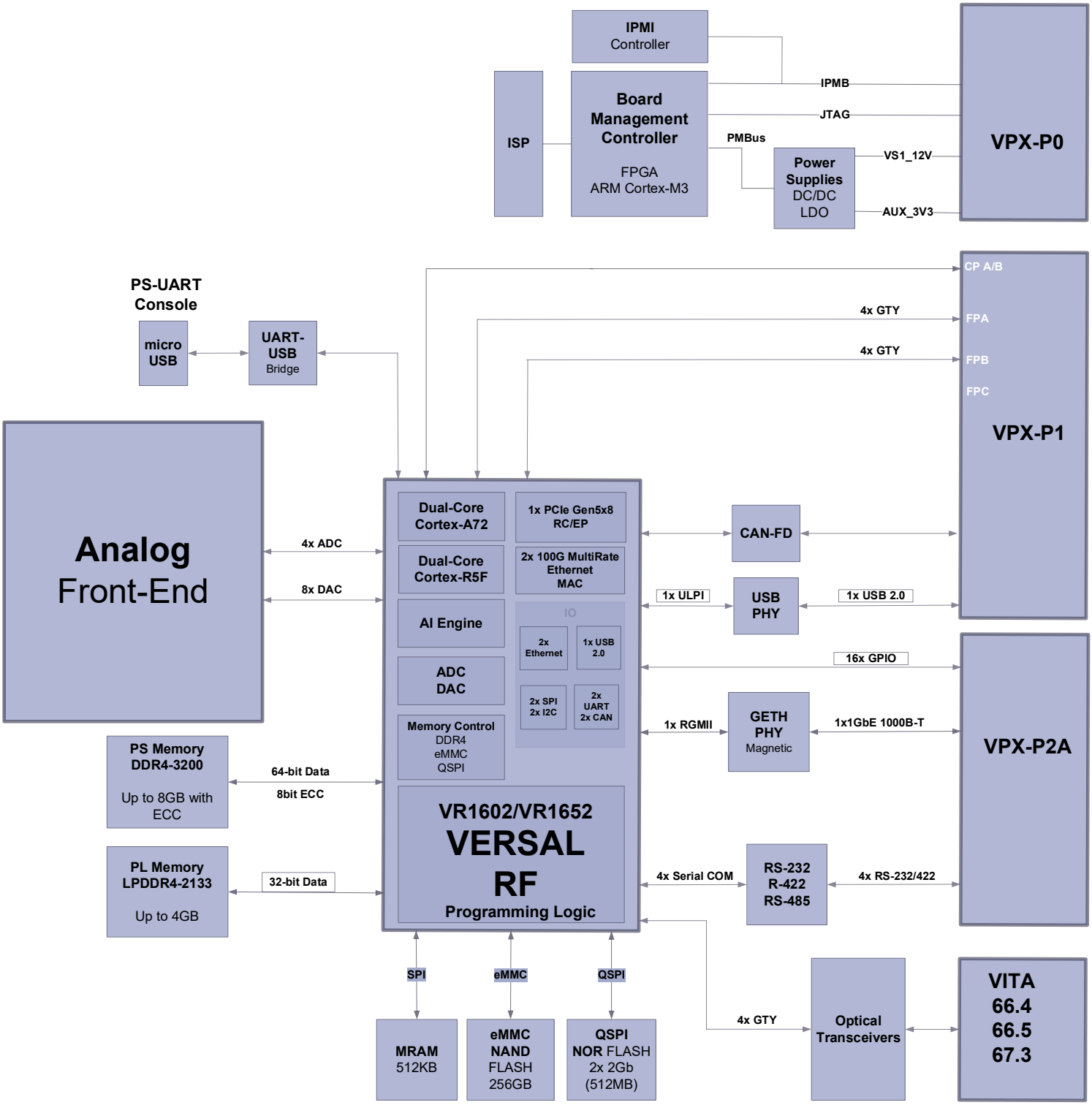
Typical Applications

- MILCOM, Software Defined Radio, MIMO
- Electromagnetic Spectrum Operations (EMSO)
- Electronic Warfare, Signal Intelligence
- LIDAR/RADAR/SONAR Systems



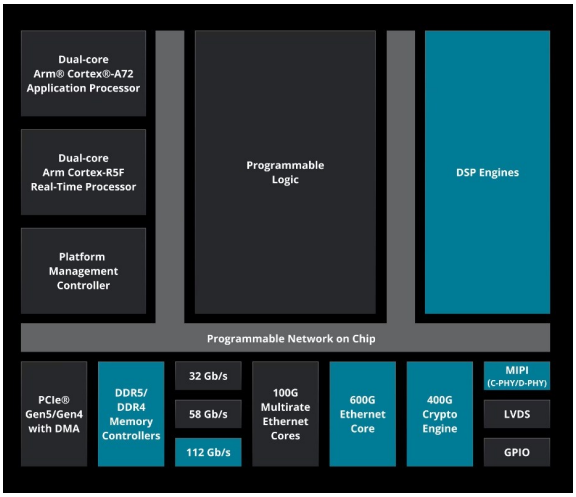
VITA Open Standards, Open Markets OpenVPX™ FMC+™

Block Diagram



AMD VERSAL Adaptative Compute Acceleration Platform (ACAP) Overview

VERSAL Prime Series Block Diagram



Architecture

Versal ACAPs are built around an integrated shell composed of a programmable network on chip (NoC), which enables seamless memory-mapped access to the full height and width of the device. ACAPs comprise: a multicore scalar processing system (PS); an integrated block for PCIe® with DMA and Cache Coherent Interconnect Designs (CPM); SIMD VLIW AI Engine accelerators for artificial intelligence and complex signal processing; and Adaptable Engines in the programmable logic (PL). Together, these form a platform for fast time-to-market (TTM) compute acceleration for cloud, edge, and networking applications. The platform management controller (PMC), adjacent to the PS, is responsible for booting and configuring the device. Versal devices typically have I/O and memory controllers on the north and south edges of the device and serial transceivers on the east and west edges. The NoC spans full height and width of the device.

Compute and Acceleration

Every Versal ACAP has Scalar Engines that comprise a dual-core Arm® Cortex®-A72 (APU) and a dual-core Arm Cortex-R5F (RPU) in the PS. The PS includes a number of peripherals for communication standards, including gigabit Ethernet and USB 2.0, and controllers for SPI, I2C, UART, and CAN-FD. The PS accesses the DDR memory controllers on the top and bottom of the device through the NoC. In addition to interfacing to external memory, the APU includes: Level 2 (L2) cache; the RPU includes tightly coupled memory (TCM); and both APU and RPU have access to the on-chip memory (OCM). The PL is made up of configurable logic blocks, containing 6-input look-up tables (LUTs) and flip-flops; different-sized memory blocks; 36Kb block RAM and 288Kb UltraRAM; digital signal processing (DSP) blocks; and a wealth of interconnect, switches, and muxes to connect blocks together. All resources are arranged in columns. The PL is divided into regions that are a fixed height. Each region has its own clocking capabilities and NoC access points.

Platform Management

The PMC resides adjacent to, but is independent from, the PS. It is responsible for the boot and configuration of the device from the primary boot source. The PMC is also responsible for configuring the PL, which can be configured before or after the PS. It also controls encryption, authentication, system monitoring, and device debug capabilities of the platform.

Connectivity

The south edge of the Versal ACAPs typically contains a number of XPIO banks and associated memory controllers to read from and write to DDR4 and LPDDR4 memory. XPIO can be used independently from the dedicated memory controllers for many functions, including any with soft memory controllers created in the PL. The east and west edges of the device typically contain serial transceivers capable of communicating up to 112Gb/s. The PL can also contain integrated blocks for high-value functions, such as the integrated block for PCIe (PL PCIE) with support for Compute Express Link (CXL), multirate Ethernet MAC, 600G Ethernet MAC, 600G Interlaken, and 400G High-Speed Crypto (HSC) Engine.

Board Specifications

3U VPX Interfaces

- VITA 46.0/46.4/46.6/65.0 VPX/OpenVPX Specifications compliant
- Optional SOSA Aligned **VPX3-VERSA-RF-AS**. Please contact us for more details
- 8x MGTY connected to/from VERSAL RF device. PCIe x4 Gen5 support
- 2x 1000BASE-X/SGMII links on VPX Control Plane
- 1x 1000BASE-T, 4x RS-232 or 2x Full-Duplex RS-422, 1x USB 2.0, 16x GPIOs, 2x CAN-FD.
- Optional 4x Full-Duplex Optical Links VITA 66.4 or 66.5. Please contact us for more details
- Optional RF VITA 67.3
- Board Management Controller (BMC) Interface. VITA 46.11 Ready
- System Controller capability
- JTAG

OpenVPX VITA 65.0 Profiles

- Optional 4x Full-Duplex Optical Links VITA 66.4. Please contact us for more details.
- Optional Front-End Connector or nanoRF VITA67.3 backplane. Please contact us for more details.

SOSA Aligned Profiles

- Please contact us for more details

AMD VERSAL RF

- Supported Devices:**VR1602** / **VR1652** VSVG1596 Package (Speed Grade –1/2)
- Processing System : Dual-Core ARM A72, Dual-Core ARM R5F, 2x USB, 2x GETH MACs
- Programmable Logic: 1205K Logic Cells / 551040 LUTs
- On-Chip Memories: 178Mb (VM1502) / 191Mb (VM1802)
- AI Engines Tiles 126 / DSP Engines: 2256
- Hard IPs: 1x PCIe Gen5x4, 2x 100G Multirate Ethernet MAC
- High Speed Serial Links:12 full duplex, high performance, GTY Multi-Gigabit Tranceivers (MGT) @ up to 32.75 Gb/s
- Supported by PanaTeQ's FPGA Development Kit

External Memories

- Up to 8GB of DDR4-3200 Processor System (PS) memory, 64-bit data, 8-bit ECC
- Up to 4GB of LPDDR4-2133 Programmable Logic (PL) memory, 32-bit data, no ECC
- 256GB eMMC of managed NAND Flash memory. HS200 support @ up to 100MB/s
- 512KB of SPI MRAM (NVRAM)
- 2x 2Gb (512MB) of QSPI NOR Flash memory for booting VERSAL Programmable Logic and Firmware Processing System

Integrated RF Subsystem

- 16x RF-ADC 14-bit 8GSPS Max Rate (VR1602). Up to 18GHz RF Input Frequency
- 4x RF-ADC 14-bit 32GSPS Max Rate (VR1652). Up to 18GHz RF Input Frequency
- 8x RF-DAC 14-bit 8GSPS Max Rate (VR1602/VR1652). RF Output Frequency

Board Management Controller (BMC)

- .Based on Microsemi SmartFusion Customizable System-on-Chip (**cSoC**) with on-chip ARM Cortex-M3 at up to 100MHz
- Real-Time Monitoring+Alarms: Voltages, Currents, Temperatures, 6-Axis Accelerometer, Magnetometer and Humidity
- Reset Management, Power-Up and Power-Down Sequencing. Buit-In Test (**BIT**)
- Watchdogs (Avionics type)
- Large private 32MB Event Log Flash Memory.
- UART communication with host using RTM-VERSA1 Rear-Transition Module
- Smart Power Management using Linear Technology DC/DC modules with Digital Power System Management.
- On-board VPX System and IPMI controllers.
- Hardware Ready for full Vita 46.11 compliance

Environnemental Specifications

- Compliant with VITA 47 specification. Please contact PanaTeQ for more information

Product Codification

The VPX3-VERSA-RF-A can be assembled with different versions of the VERSAL RF devices and various amounts of memory storage. The cooling technique et ruggedization level are also available options. The following table shows the product coding for all these options.

VPX3-VERSA-RF-A- a b c – rl – d – e-k

a	Zynq RFSoC Device	RF-ADC 14-bit 8GSPS	RF-ADC 14-bit 32GSPS	RF-DAC 14-bit 16GSPS	GTY	Logic Cells	DSP Slices	AI Engines	Memory
A	VR1602	16	0	8	12	1205K	2256	126	156 Mb
B	VR1652	0	4	8	12	1205K	2256	126	156 Mb

b	Device Speed
1	Standard
2	Faster

c	PS / PL DDR4 Memory
N	4GB / 2GB
M	8GB / 2GB

rl	Ruggedization Level	Vita 47
AS	Air Standard	EAC4
AR	Air Rugged	EAC6
CC	Conduction Cooled	ECC3

d	RF I/O	Optical
A	Front Panel	None
B	Front Panel	Rear 66.4
C	Rear 67.3	N/A
D	Rear 67.3	Rear 66.4

e	Option
E	Conformal Coating

k	VPX connectors
K	KVPX Connectors

Ordering Information

Reference	Description
RTM-VERSA-RF-A	Rear Transition Module for VPX3-VERSA-RF-A
VPX3-VERSA-RF-A-PSDK	VPX3-VERSA-RF-A System Development Kit

The following product references are offered by Panateq as standard products. Other combinations of devices, speed grade, memory and cooling can be specially ordered. Please contact us for details

Reference	Device	Speed Grade	Memory PS/PL	Ruggedization Level
VPX3-VERSA-RF-A-B1M-AS	VR1652	-1	8GB/2GB	Standard Air Cooled

PanaTeQ Advanced Engineering

PanaTeQ Contact

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Available from: